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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/820,374	03/12/1997	Cheol-sung Hwang	SEC.314	2825
20987	7590	05/04/2006	EXAMINER	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190				DICKEY, THOMAS L
		ART UNIT		PAPER NUMBER
		2826		

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

(b) /

Office Action Summary	Application No.	Applicant(s)
	08/820,374	HWANG, CHEOL-SUNG
	Examiner	Art Unit
	Thomas L. Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 April 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 25-28 and 30-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 36-45 is/are allowed.
- 6) Claim(s) 25-28 and 30-34 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 12 March 1997 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 08/560,087.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/10/06 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 25-28 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over SUMMERFELT ET AL. (5,566,045) in view of PARK (5,774,327).

A. With regard to claims 25-28 the Figure 23 embodiment of Summerfelt et al. discloses a lower electrode of a capacitor in a semiconductor device, comprising a first layer 34 comprising TiN (note Table, column 12), a material that serves as a barrier

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against the diffusion of impurities from a lower substrate 32; a second layer 66 formed over the first layer 34, the second layer 66 may comprise RuO₂ (note the table entry for layer 66), a material that is, by applicants' admission, easy to pattern; and a third layer 68 formed over top and side surfaces of the second layer 66 and side surfaces of the first layer 34, the third layer 68 may comprise Pt (note the table entry for layer 68), a material having, by applicants' admission, low leakage current properties. Summerfelt et al. does not disclose that the lower substrate exposed by third layer is overetched.

However, Park discloses a lower electrode of a capacitor comprising a first layer 31A in the form of a plate comprising a material (TiN) that serves as a barrier against the diffusion of impurities from a lower substrate 36; and a third layer 32A formed over top and side surfaces of the second layer and side surfaces of the first layer 31A, the third layer 32A comprising a material (Pt) having low leakage current properties wherein the lower substrate 36 exposed by third layer 32A is overetched (indicated by circle "B" in figure 9). Note figures 6-9 and column 5 line 18 through column 6 line 27 of Park. Park also discloses two elements not found in Applicant's claims: a capacitor dielectric 33A and a double layered upper electrode 34A-44A. According to Park, overetching of lower substrate 36 is necessary in order to assure proper electrical contact between the layers of the upper electrode. Note column 6 lines 16-20 of Park. Therefore, it would have been obvious to a person having skill in the art to overetch the lower substrate of Summerfelt et al.'s lower electrode, as is taught by Park, in order to fully expose one

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layer of an upper electrode of a capacitor to another layer of said upper electrode to thus provide better grounding of the upper electrode.

B. With regard to claims 30-34 the Figure 23 embodiment of Summerfelt et al. discloses a semiconductor device, comprising an insulating (note Table, column 10) film 32 formed over a semiconductor (note Table, column 11) substrate 30; a polysilicon (note Table, column 12) conductive plug 52 formed in the insulating film 32; a first layer 34 formed over the conductive plug 52 and the insulating film 32, the first layer 34 comprising TiN (note Table, column 12), a material that serves as a barrier against the diffusion of impurities from the conductive plug 52 and the semiconductor substrate 30; a second layer 66 formed over the first layer 34, the second layer 66 may comprise RuO₂ (note the table entry for layer 66), a material that is, by applicants' admission, easy to pattern; and a third layer 68 formed over top and side surfaces of the second layer 66 and side surfaces of the first layer 68 may comprise Pt (note the table entry for layer 68), a material having, by applicants' admission, low leakage current properties. Summerfelt et al. does not disclose that the insulating film exposed by the third layer is overetched.

However, Park discloses a semiconductor device, comprising an insulating film 26-36 formed over a semiconductor substrate 10; a polysilicon conductive plug 28 formed in the insulating film 26-36; a first layer 31A formed over the conductive plug 28 and the insulating film 26-36, the first layer 31A comprising a material (TiN) that serves as a

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barrier against the diffusion of impurities from the conductive plug 28 and the semiconductor substrate 10; and a third layer 32A formed over top and side surfaces of the second layer and side surfaces of the first layer 31A, the third layer 32A comprising a material having low leakage current properties; wherein the insulating film 26-36 exposed by the third layer 32A is overetched (indicated by circle "B" in figure 9). Note figures 6-9 and column 5 line 18 through column 6 line 27 of Park. Park also discloses two elements not found in Applicant's claims: a capacitor dielectric 33A and a double layered upper electrode 34A-44A. According to Park, overetching of insulating film 26-36 is necessary in order to assure proper electrical contact between the layers of the upper electrode. Note column 6 lines 16-20 of Park. Therefore, it would have been obvious to a person having skill in the art to overetch the insulating film of Summerfelt et al.'s semiconductor device, as is taught by Park, in order to fully expose one layer of an upper electrode of a capacitor to another layer of said upper electrode to thus provide better grounding of the upper electrode.

Response to Arguments

3. Applicant's arguments with respect to claims 25-28 and 30-34 have been considered but are moot in view of the new ground(s) of rejection.

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Allowable Subject Matter

4. Claims 36-45 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as, inter alia, a third, low leakage current electrode layer disposed on top and side surfaces of a second, easily patterned electrode layer and on exposed side surfaces of a first, barrier electrode layer formed under the second electrode layer, with the second layer not completely covering the first layer but rather exposing said first layer side surfaces, as recited in claims 36 and 45.

Note that the figure 23 embodiment of Summerfelt et al. discloses all the limitations of claims 36 and 40 except that Summerfelt et al.'s second layer does not expose the side surfaces of Summerfelt et al.'s first layer.

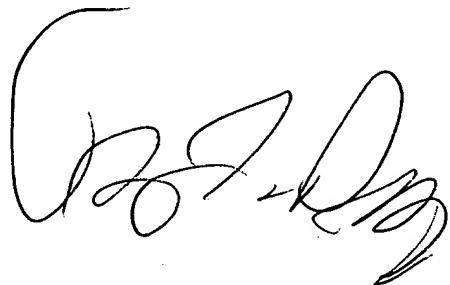
Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
04/06